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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,850	12/02/2003	Joel P. de Souza	YOR920030602US1 (17242)	3232

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,850	DE SOUZA ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-57 and 59-79* is/are pending in the application.

4a) Of the above claim(s) *35-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *56,57 and 59-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 01/23/2006, claims 35-57, and 59-79 are active in this application.

Claims 35-55 have been withdrawn.

Claims 1-34, 58, and 80 have been cancelled.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 10/11/2005. The references cited on the PTOL 1449 form have been considered.

Election/Restriction

3. This application contains claim(s) 35-55 drawn to an invention nonelected without traverse in the reply filed on 09/26/2005. A complete reply to the **final rejection** must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Also, upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently

named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

Claim Objection

4. The claim is objected to for the following reason: Claim 68 originally depends on claim 58. However, claim 58 has been cancelled. Therefore, the dependency of claim 68 must be corrected. Appropriate correction is required.

Remarks

5. Applicant's argument(s), filed 01/23/2006, with respect to claims 56, 57, and 59-79 have been fully considered, but they are not persuasive.

First, with respect to the reference of Alki et al., Examiner do/does not agree with Applicant that Alki et al. do not disclose a structure including a first single crystal semiconductor region and a second single crystal semiconductor region that are both disposed on a common buried insulating layer which lays atop a substrate. Col. 3, lines 1-6 teaches that the device of Ali et al. is an SOI integrated circuit, which means that the device of Alki is formed by using a silicon-on-insulator substrate. Therefore, it is clear that the semiconductor layer 60 of Alki is formed on an insulator layer that lays atop a substrate.

Second, with respect to the teaching of AAPA, Examiner do/does not agree with Applicant that AAPA does not disclose a structure including a first single crystal semiconductor region and a second single crystal semiconductor region that are both disposed on a common buried insulating layer which lays atop a substrate, nor a structure including one single semiconductor region and at least one bilayer semiconductor region are both disposed on a common buried insulating layer, said insulating layer is located on a substrate. Fig. 4 of AAPA clearly shows that all of layers 320 and 430 are disposed on the buried oxide layer 420 which is formed on the substrate 410. Clearly, AAPA does disclose all of the above claimed limitations.

For the above reasons, it is believed that the previous Office Action should be retained and rewritten as follow in corresponding to the amended claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim(s) 56 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 4,768,076, to Aoki et al.

Regarding claim 56, Aoki discloses a planar hybrid-orientation semiconductor substrate structure, as shown in figs. 5, 7, 10, comprising:

at least one clearly defined first single crystal semiconductor region 10 having a first surface crystal orientation (110) and at least one clearly defined second single crystal semiconductor region 18 having a second surface crystal orientation (100) different from the first, said second semiconductor regions 18 formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation (100) and said first single crystal semiconductor region 10 and said second single crystal semiconductor region 18 are both disposed on a common buried insulating layer that lays atop a substrate (SOI substrate discussed on col. 3, lines 1-6). See also col. 5, line 1 to col. 6, line 45 and the above remark.

Nevertheless, the limitation(s) "said second semiconductor regions formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation" is process limitation(s), and the discussed claim is drawing to a product. The process limitation(s) of how the second semiconductor regions being formed has/have no patentable weight in claim drawn to structure. Note that a "product by process" claim is directed to the product per

se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue) and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. MPEP §2113 states that "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)."

Therefore, the recitation "said second semiconductor regions formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation" is considered a process of making product and has been given no patentable weigtht in a product-by-process claim and is thus non-limiting.

8. Claim(s) 56, 57, 59-69 and 72-79 are rejected under 35 U. S. C. § 102 (b) as being anticipated by admitted prior art (Admission).

Regarding claim 56, Admission discloses a planar hybrid-orientation semiconductor substrate structure, as shown in figs. 1-4 of the instant application, comprising:

at least one clearly defined first single crystal semiconductor region 320 having a first surface crystal orientation (100) and at least one clearly defined second single crystal semiconductor region 440 having a second surface crystal orientation (110) different from the first, said second semiconductor regions formed by amorphizing a semiconductor material 430 having said first orientation and recrystallizing it into a semiconductor material having said second orientation (110) and said first single crystal semiconductor region 320 and said second single crystal semiconductor region 440 are both disposed on a common buried insulating layer 420 that lays atop a substrate 410. See further the instant specification, pages 2-3, and the above remark.

Nevertheless, the limitation(s) "said second semiconductor regions formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation" is process limitation(s), and the discussed claim is drawing to a product. The process limitation(s) of how the second semiconductor regions being formed has/have no patentable weight in claim drawn to structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also

In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue) and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. MPEP §2113 states that "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)."

Therefore, the recitation "said second semiconductor regions formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation" is considered a process of making product and has been given no patentable weigtht in a product-by-process claim and is thus non-limiting.

Regarding claim 57, Admission discloses the hybrid-orientation substrate structure further comprising at least one isolation region 330 separating said at least one first single crystal semiconductor region 320 from said at least one second single crystal semiconductor region 440. See figs. 1-4.

Regarding claim 59, Admission discloses the planar hybrid-orientation substrate structure wherein said at least one isolation region comprises a dielectric-filled trench. See figs. 1-4, and pages 2-3 of the instant specification.

Regarding claim 60, Admission discloses the planar hybrid-orientation substrate structure wherein materials of said first and second semiconductor regions are selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloy thereof, and other III-V or II-VI compound semiconductors. See the specification, pages 2-3 of the instant application.

Regarding claims 61-62, Admission discloses the planar hybrid-orientation substrate structure comprising all claimed limitations. See the specification, page 2-3 of the pending application.

Regarding claim 63, Admission discloses the hybrid-orientation substrate structure wherein said different surface crystal orientations are selected from the group

consisting of (110), (111) and (100). See the specification, page 2-3 of the pending application.

Regarding claim 64, Admission discloses the planar hybrid-orientation substrate structure wherein said first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation. See the specification, page 2-3 of the pending application.

Regarding claim 65, Admission discloses the planar hybrid-orientation substrate structure wherein one of said semiconductor regions has a (110) crystal orientation (first semiconductor region 320) and said other semiconductor region 440 has a (100) crystal orientation. See the specification, page 2-3 of the pending application.

Regarding claim 66, Admission discloses the planar hybrid-orientation substrate structure further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a (100) crystal orientation and said at least pFET device is located on a (110) crystal orientation. See the specification, page 2-3 of the pending application.

Regarding claims 67-68, Admission discloses the planar hybrid-orientation substrate structure comprising all claimed limitations See the specification, page 2-3 of the pending application.

Regarding claim 69, Admission discloses a planar hybrid-orientation semiconductor-on-insulator (SOI) substrate structure, as shown in figs. 1-4 of the instant application, comprising at least one single-layer semiconductor region 440 comprising a semiconductor having a first single-crystal surface orientation and at least one bilayer semiconductor region 320/430 comprising a lower semiconductor layer 430 having said first single crystal surface orientation and an upper semiconductor layer 320 having a second single crystal surface orientation different from the first, wherein said at least one single semiconductor region 440 and said at least one bilayer semiconductor region 320/430 are both disposed on a common buried insulating layer 420, said insulating layer 420 is located on a substrate 410. See further the specification, page 2-3 of the pending application, and the above remark.

Regarding claim 72, Admission discloses the structure wherein said common buried insulator layer 420 is a dielectric material selected from the group consisting of SiO2, SiO2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials. See the specification, page 2-3 of the pending application.

Regarding claims 73-75, Admission discloses the hybrid-orientation substrate structure comprising all claimed limitations. See further the specification, page 2-3 of the pending application.

Regarding claim 76, Admission discloses the hybrid-orientation SOI substrate structure further comprising at least one nFET device and at least one PFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said nFET device and wherein said at least pFET device is locate on a crystal orientation that is optimal for said pFET device. See the specification, page 2-3 of the pending application.

Regarding claim 77, Admission discloses the planar hybrid-orientation SOI substrate structure wherein said different surface orientations are selected from the group consisting of (110), (111) and (100). See further the specification, page 2-3 of the pending application.

Regarding claims 78-79, Admission discloses the hybrid-orientation substrate structure comprising all claimed limitations. See further the specification, page 2-3 of the pending application.

Claim Rejections - 35 U.S.C. § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to

a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim(s) 70 and 71 are rejected under 35 U.S.C. 103 (a) as being unpatentable over admitted prior art (Admission) in view of the following remarks.

Regarding claims 70 and 71, Admission discloses the structure further including at least one isolation region 330. The isolation region 330 shown in figs. 3-4 just partially separating said at least one single-layer semiconductor region from said at least one bilayer semiconductor region. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the isolation region 330 so that it would extend to and/or even under the buried oxide and deep into the substrate, as that shown in figs. 1c-d. Such modification would not change the scope and/or spirit of the invention illustrated by fig. 4, and that such modification would involve only routine skills in the art as it is taught by figs. 1c-d.

Conclusion

11. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the

statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
March 22, 2006